NEC

TFT COLOR LCD MODULE

NL10276AC30-07
38cm (15 Type), XGA

PRELIMINARY DATA SHEET

(4th Edition)

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Approved by	*Date* June 12, 2001
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Prepared by	*Date* June 12, 2001

INTRODUCTION

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Anti-radioactive design is not implemented in this product.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL10276AC30-07 module is composed of the driver LSIs for driving the TFT (Thin Film Transistor) array with an amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into the narrow gap between a TFT array glass substrate and a color filter glass substrate.

RGB (Red, Green, Blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn address the individual TFT cells.

Working as an electro-optical switch, each TFT cell regulates transmitted light from the backlight assembly when worked by the data source. Color images are created by regulating the amount of transmitted light through the array of red, green and blue dots.

1.2 APPLICATIONS

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- FA monitor

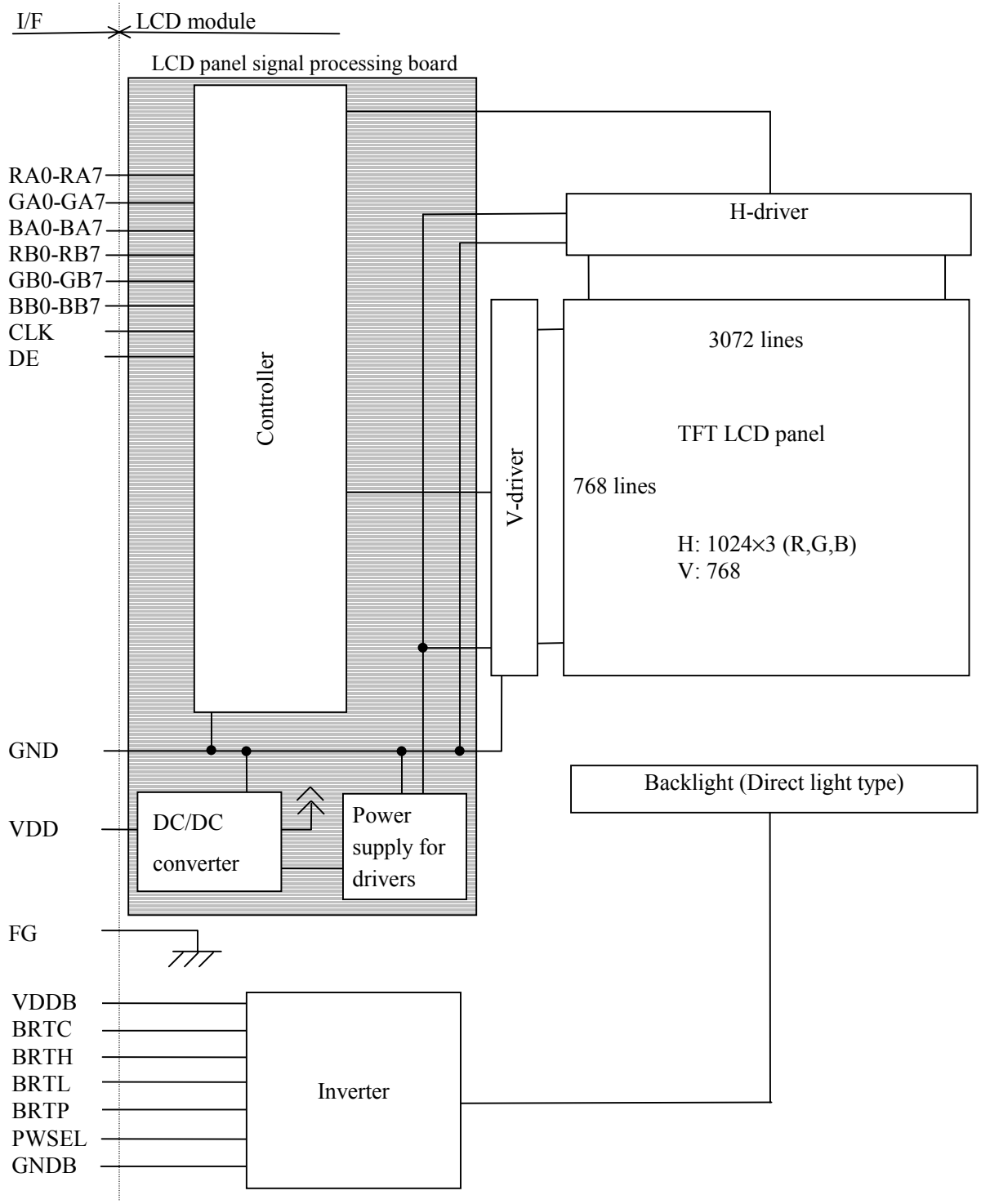
1.3 FEATURES

- Parallel 8bit interface (2 port)
- Ultra-wide viewing angle (with lateral electric field)
- Fast response time
- High luminance
- High contrast
- Wide color gamut
- Luminance control
- Small foot print
- Direct light type
- Replaceable backlight unit and inverter

2. GENERAL SPECIFICATIONS

Display area	304.128 (H) × 228.096 (V) mm	
Diagonal size of display	38 cm (15.0 inches)	
Drive system	a-Si TFT active matrix	
Display colors	16,777,216 colors (6bit + FRC)	
Number of pixels	1024 (H) × 768 (V) pixel	
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	
Dot pitch	0.099 (H) × 0.297 (V) mm	
Pixel pitch	0.297 (H) × 0.297 (V) mm	
Module size	330.0 (H) × 256.0 (V) × 30.0 Max.(D) mm	4
Weight	1100 g (Typ.)	4
Contrast ratio	300:1 (Typ.)	
Viewing angle (To be out of 10:1 for the contrast ratio)	• Horizontal: 85° (Typ. , left side, right side) • Vertical: 85° (Typ. , up side, down side)	
Designed viewing direction	• Optimum grayscale (γ=2.2): perpendicular	
Polarizer pencil-hardness	2H (Min., at JIS K5400)	
Color gamut	60 % (Typ.) At center, to NTSC	
Response time	Ton =10 ms (Typ.,10%→90%)	4
Luminance	400 cd/m^2 (Typ.)	4
Signal system	Parallel 8bit interface (2port) [RGB 8bit data, CLK, DE]	
Supply voltage	5V (for LCD panel signal processing board) 12V (for Backlight inverter)	
Backlight	Direct light type: 8 cold cathode fluorescent lamps [Replaceable parts] • Backlight unit: TBD • Inverter: TBD	
Power consumption	24 W (Typ.) (Checkered flag pattern, at 400 cd/m^2 Typ.)	

3. BLOCK DIAGRAM



Note1: GND is connected to FG (Frame Ground) in the LCD module. Neither GND nor FG is connected to GNDB (Backlight Ground). These grounds should be connected to system ground in customer equipment. ⚠4

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	330.0 ± 1.0 (H) × 256.0 ± 1.0 (V) × 30.0 Max. (D) Note1	mm
Display area	304.128 ± 0.5 (H) × 228.096 ± 0.5 (V) Note1	mm
Weight	1,100 (Typ.), 1200 (Max.)	g

Note1: See "**11.OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameters		Symbol	Rating	Unit	Remarks
Supply voltage	LCD panel signal board	VDD	-0.3 to +6.0	V	Ta = 25°C
	Inverter	VDDB	-0.3 to +15.0	V	
Input voltage	Display signals Note3	Vi	-0.3 to +3.8	V	Ta = 25°C VDD=5.0V
	BRTC	ViB1	-0.3 to +5.5	V	Ta = 25°C VDDB=12V
	BRTP	ViB2	-0.3 to +5.5	V	
	PWSEL	ViB3	-0.3 to +5.5	V	
	ACA	ViB4	-0.3 to +5.5	V	
	BRTL	ViB5	-0.3 to +1.5	V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature		Top1	0 to +55		Module front surface Note1
		Top2	TBD		Module rear surface Note2
Relative humidity (RH) Note4			≤ 95	%	Ta≤ 40°C
			≤ 85		40°C <Ta≤ 50°C
			≤ 70		50°C <Ta≤ 55°C
Absolute humidity Note4			≤ 78 Note5	g/m^3	Ta>55°C
Operating altitude			≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude			≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: Measure at the display area
Note2: Measure at the rear shield
Note3: Display signals are DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7
Note4: No condensation
Note5: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage		VDD	4.5	5.0	5.5	V	-
Supply current		IDD	-	300 Note1	600 Note2	mA	VDD=5.0V
Ripple voltage		VRP	-	-	100	mV	VDD=5.0V
Logic input voltage	Low	VTL	0	-	0.8	V	-
Logic input voltage	High	VTH	2.0	-	3.6	V	

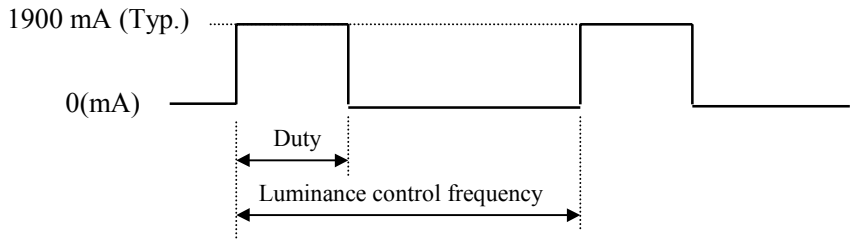
Note1: Checker flag pattern (in EIAJ ED-2522)
Note2: Theoretical maximum current pattern

4.3.2 Driving for backlight inverter

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage		VDDB	11.4	12.0	12.6	V	Backlight power supply
Supply current	Note1	IDDB	-	1900	2100	mA	VDDB=12.0V (at Max. luminance)
Logic input voltage	BRTC	ViBL1	0	-	0.8	V	-
		ViBH1	2.0	-	5.0	V	
	BRTP	ViBL2	0	-	0.8	V	-
		ViBH2	2.0	-	5.0	V	
	PWSEL	ViBL3	0	-	0.8	V	-
		ViBH3	2.0	-	5.0	V	
	ACA	ViBL4	0	-	0.8	V	-
		ViBH4	2.0	-	5.0	V	
Logic input current	BRTC	IiBL1	-610	-	-	µA	-
		IiBH1	-	-	440	µA	
	BRTP	IiBL2	-1580	-	-	µA	-
		IiBH2	-	-	3500	µA	
	PWSEL	IiBL3	-610	-	-	µA	-
		IiBH3	-	-	440	µA	
	ACA	IiBL4	-810	-	-	µA	-
		IiBH4	-	-	440	µA	
BRTL input current	BRTL	IiB5	-130	-	-	µA	-

Note1: Inverter current wave is as follows.



Maximum luminance control : 100% (Duty)
Minimum luminance control : 20% (Duty)
Luminance control frequency : 285±14 Hz (Typ.) 4

Luminance control frequency indicate the input pulse frequency, when select the luminance control with external pulse. See "**4.6.2 Luminance control with external pulse** ".

4.3.3 Supply voltage ripple

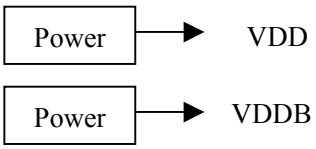
This module works, even if the ripple levels are beyond the below values (See following the table.), but might have noise on the display image. Consider and evaluate enough before installing this module into customer's system.

Supply voltage (Acceptable level)	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD (for LCD panel signal processing board; 5.0V)	≤ 100	mVp-p
VDDB (for backlight inverter; 12V)	≤ 200	mVp-p

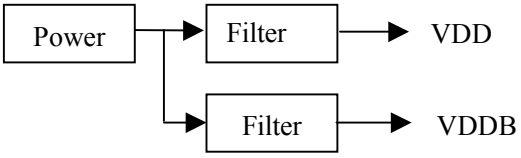
Note1: The acceptable ripple voltage level includes spike noise.

Example of the power supply connections

a) Separate the power supply



b) Put in the filters



4.3.4 Fuses

This module has fuses listed below. Check and evaluate power supplies of customer's system.

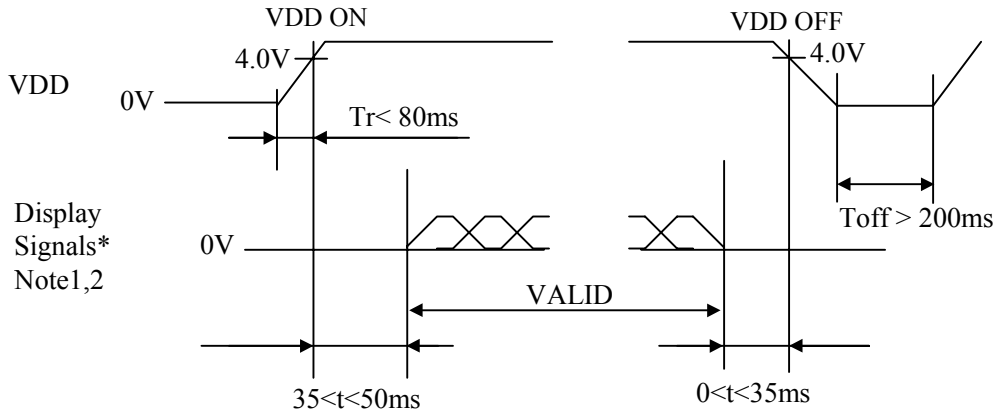
Fuse		Rating Note1	Unit	Remarks
Type	Supplier			
FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2	A	VDD (for LCD panel signal processing board)
KE40	Daito Communication Apparatus Co,. Ltd	4	A	VDDB (for backlight inverter)

4

Note1: The power capacity should be more than 2 times of fuse ratings from safety point of view. If the power capacity of customer system is less than above request, check and evaluate it carefully.

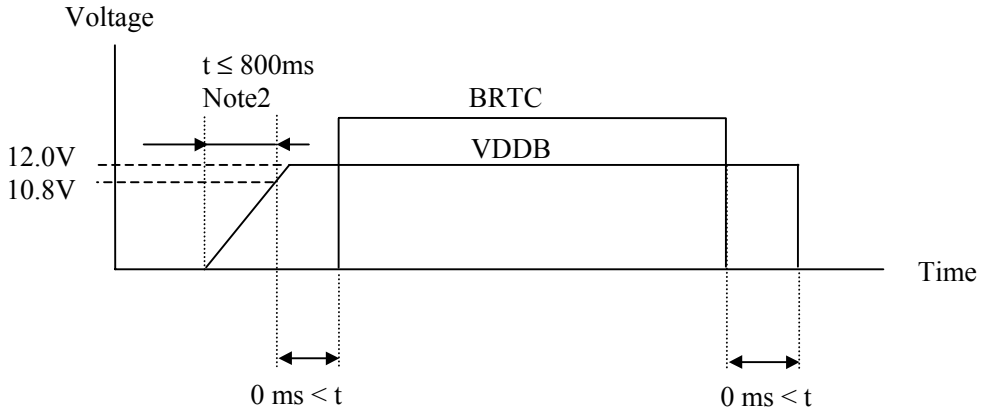
4.4 SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board



Note1: Display signals (DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7) must be "0" voltage (V), exclude the VALID period (See above sequence diagram). If input voltage to display signals is higher than 0.3V, the internal circuits might be damaged.
Note2: The values of signals are measured at the termination resistor of 100 ohm.
Note3: In terms of fall-off-potential while VDD leading edge is below 4.0V, protection circuits may work and then the module may not work.
Note4: If display signals to this module are cut while this module is working, even if the signal input to it once again, it may not work normally.

4.4.2 Sequence for backlight inverter



Note1: Backlight ON/OFF should be controlled, while display signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data may be displayed when the backlight power is turned ON/OFF during display signals out.
Note2: Only when BRTC is Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

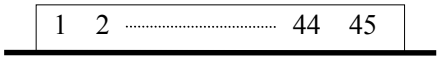
4.5.1 LCD panel signal processing board

CN1 socket (Module side): IL-FHR-F45S-HF (JAE) or FH12S-45S-0.5SH (HIROSE) ⚠4

Pin No.	Symbol	Function	Description
1	GND	Ground	Connect to system ground.
2	CLK	Dot clock	Dot clock input
3	GND	Ground	Connect to system ground.
4	DE	Data enable	Data enable input
5	GND	Ground	Connect to system ground.
6	N.C.	Non-connection	Keep the terminal open
7	GND	Ground	Connect to system ground.
8	N.C.	Non-connection	Keep the terminal open
9	GND	Ground	Connect to system ground.
10	N.C.	Non-connection	Keep the terminal open
11	GND	Ground	Connect to system ground.
12	BA7	Odd pixel data B	Odd pixel data B input BA7: Most significant bit
13	BA6		
14	BA5		
15	BA4		
16	GND	Ground	Connect to system ground.
17	BA3	Odd pixel data B	Odd pixel data B input BA0: Least significant bit
18	BA2		
19	BA1		
20	BA0		
21	GND	Ground	Connect to system ground.
22	GA7	Odd pixel data G	Odd pixel data G input GA7: Most significant bit
23	GA6		
24	GA5		
25	GA4		
26	GND	Ground	Connect to system ground.
27	GA3	Odd pixel data G	Odd pixel data G input GA0: Least significant bit
28	GA2		
29	GA1		
30	GA0		
31	GND	Ground	Connect to system ground.
32	RA7	Odd pixel data R	Odd pixel data R input RA7: Most significant bit
33	RA6		
34	RA5		
35	RA4		
36	GND	Ground	Connect to system ground.
37	RA3	Odd pixel data R	Odd pixel data R input RA0: Least significant bit
38	RA2		
39	RA1		
40	RA0		
41	VDD	Power Supply	+5V±10%
42	VDD		
43	VDD		
44	VDD		
45	N.C.	Non-connection	Keep the terminal open

Note1: Do not keep pins free (except N.C. Pin) to avoid noise issue.

CN1 socket: Figure of socket

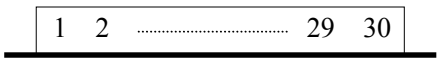


CN2 socket (Module side): IL-FHR-F30S-HF (JAE) or FH12S-30S-0.5SH (HIROSE)

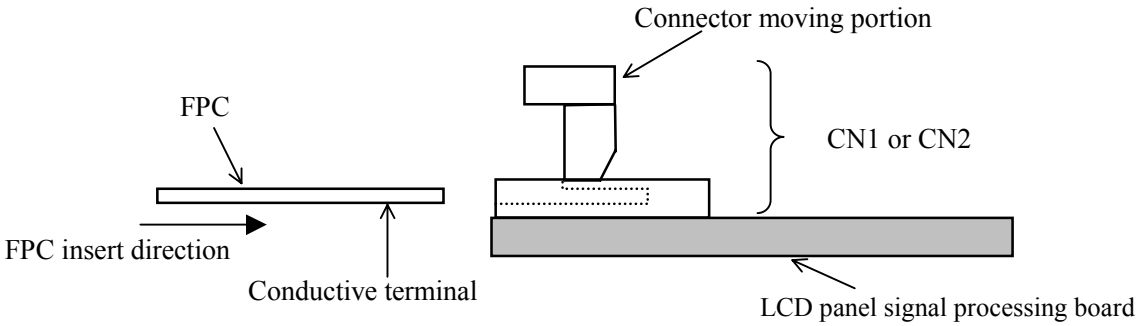
Pin No.	Symbol	Function	Description
1	GND	Ground	Connect to system ground.
2	BB7	Even pixel data B	Even pixel data B input BB7: Most significant bit
3	BB6		
4	BB5		
5	BB4		
6	GND	Ground	Connect to system ground.
7	BB3	Even pixel data B	Even pixel data B input BB0: Least significant bit
8	BB2		
9	BB1		
10	BB0		
11	GND	Ground	Connect to system ground.
12	GB7	Even pixel data G	Even pixel data G input GB7: Most significant bit
13	GB6		
14	GB5		
15	GB4		
16	GND	Ground	Connect to system ground.
17	GB3	Even pixel data G	Even pixel data G input GB0: Least significant bit
18	GB2		
19	GB1		
20	GB0		
21	GND	Ground	Connect to system ground.
22	RB7	Even pixel data R	Even pixel data R input RB7: Most significant bit
23	RB6		
24	RB5		
25	RB4		
26	GND	Ground	Connect to system ground.
27	RB3	Even pixel data R	Even pixel data R input RB0: Least significant bit
28	RB2		
29	RB1		
30	RB0		

Note1: Do not keep pins free to avoid noise issue.

CN2 socket: Figure of socket



Note2: Insert the FPC into the CN1 and CN2 with conductive terminal down.



Sectional drawing of CN1 and CN2

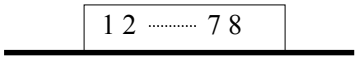
4.5.2 Backlight inverter

CN201 socket (Module side): DF3-8P-2H (HIROSE ELECRIC Co., Ltd.)
Adaptable plug: TBD

Pin No.	Symbol	Function	Description
1	GNDB	Ground for backlight	Connect to system ground.
2	GNDB		
3	GNDB		
4	GNDB		
5	VDDB	Power supply for backlight	+12V±5%
6	VDDB		
7	VDDB		
8	VDDB		

Note1: Do not keep pins free to avoid noise issue.

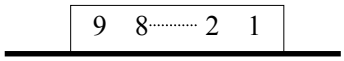
CN201 socket: Figure of socket



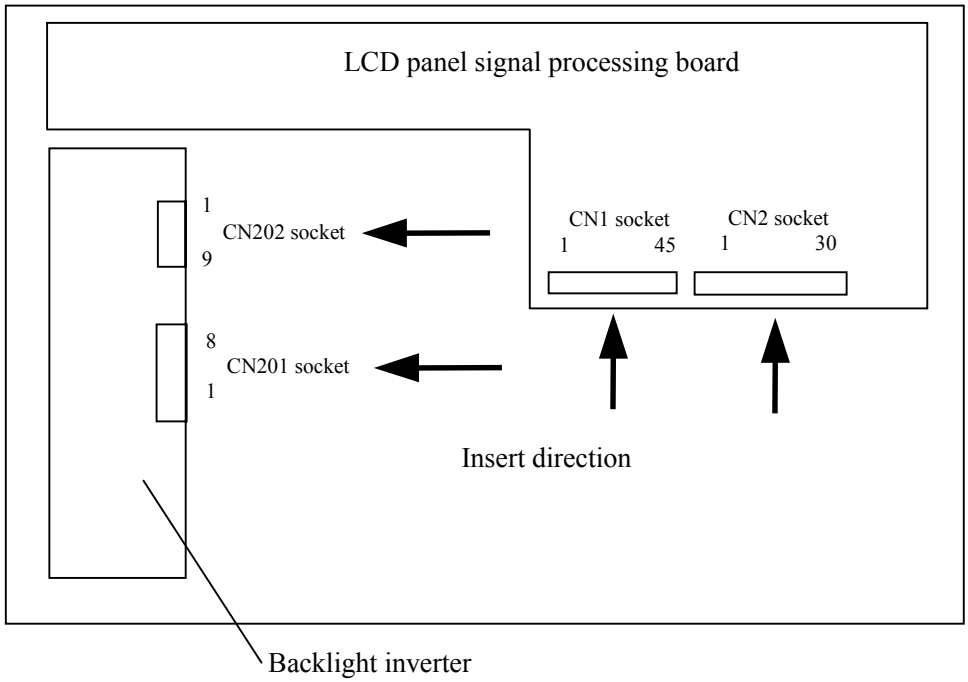
CN202 socket (Module side): IL-Z-9PL1-SMTY(JAE)
Adaptable plug: TBD

Pin No.	Symbol	Function	Description
1	GNDB	Ground for backlight	Connect to system ground.
2	GNDB		
3	ACA	Luminance control signal	"High" or "Open" : Normal luminance 100% "Low" : Low luminance (TBD%)
4	BRTC	Backlight ON/OFF control signal	"High" or "Open" : Backlight ON "Low" : Backlight OFF
5	BRTH	Luminance control signal	See "**4.6 LUMINANCE CONTROLS**".
6	BRTL		
7	BRTP		
8	GNDB	Ground for backlight	Connect to system ground.
9	PWSEL	Luminance control select signal	See "**4.6 LUMINANCE CONTROLS**".

CN202 socket: Figure from socket view

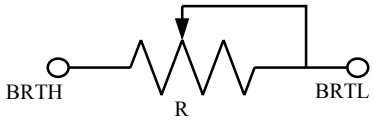


4.5.3 Position of sockets



4.6 LUMINANCE CONTROLS

4.6.1 Luminance control method

Control method	Function and adjustment	PWSEL	BRTP
PWM	Luminance controlled by BRTP signal. See "**4.6.2 Luminance control with external luminance**".	Low	Input
Variable resistor Note1	The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor corresponds to the minimum of luminance.  Max. luminance (TBD%): R=10kΩ Min. luminance (TBD%): R=0Ω Mating variable resistor: 10kΩ ±5%, B curve, 1/10W	High or Open	Open
Voltage Note1	BRTH should be fixed to 0V, and input to BRTL as follows. Max. Luminance (TBD%): 1V(Typ.) Min. Luminance (TBD%): 0V		

Note1: Luminance control may be overlap noises on the display image depending on input signal timing. In this case, keep off the interference between input signal and backlight driving signal, by PWM (Pulse Width Modulation) method.

4.6.2 Luminance control with external pulse

Luminance control with external pulse activated when PWSEL is Low and external pulse signal is inputted to BRTP. This luminance control is controlled by duty ratio, and luminance is as follows.

Duty ratio=100%: Max. luminance

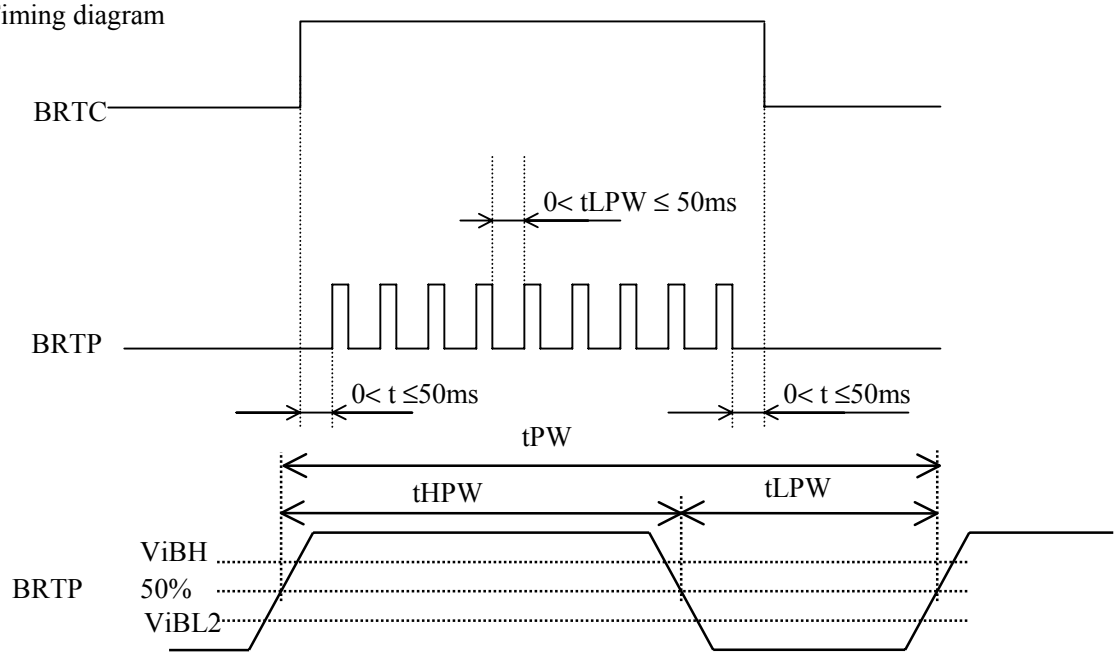
Duty ratio=30%: Min. luminance

In case of BRTC = High or Open, the inverter will stop working when BRTP terminal is fixed to Low in the condition of PWSEL = Low. In this case, backlight will not turn on, even if external pulse signal is inputted to BRTP again. This is not out of order. Inverter will start to work when power is supplied again.

The display image may be disturbed by luminance control with external pulse when set up frequency is interfered with internal signal frequency.

External pulse timing (PWSEL = Low)

- Timing diagram



- Each parameter

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input pulse frequency		1/tPW	185	-	325	Hz	Note1
Low period		tLPW	-	-	50	ms	Note2
Duty ratio		tHPW/tPW	20	-	100	%	Note3
Luminance ratio		-	-	30-100	-	%	-
Input voltage	Low	ViBL2	0	-	0.8	V	-
	High	ViBH2	2.0	-	5.0	V	-

Note1: See the following formula for luminance control frequency.
Luminance control frequency = Vsync frequency × (n+0.25) [or (n + 0.75)]
Note2: In case tLPW is out of 50ms, backlight will turn off by its protection circuits.
Note3: Max. Luminance at 100%

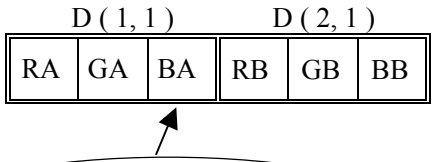
4.7 DISPLAY COLORS TO INPUT DATA SIGNALS

Display color		Data signal (0: Low level, 1: High level)																									
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:								:								:				
	↓				:								:								:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note1: Colors are developed in combination with 8-bit signals (256 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 16,777,216 (256×256×256) colors.

4.8 DISPLAY POSITIONS

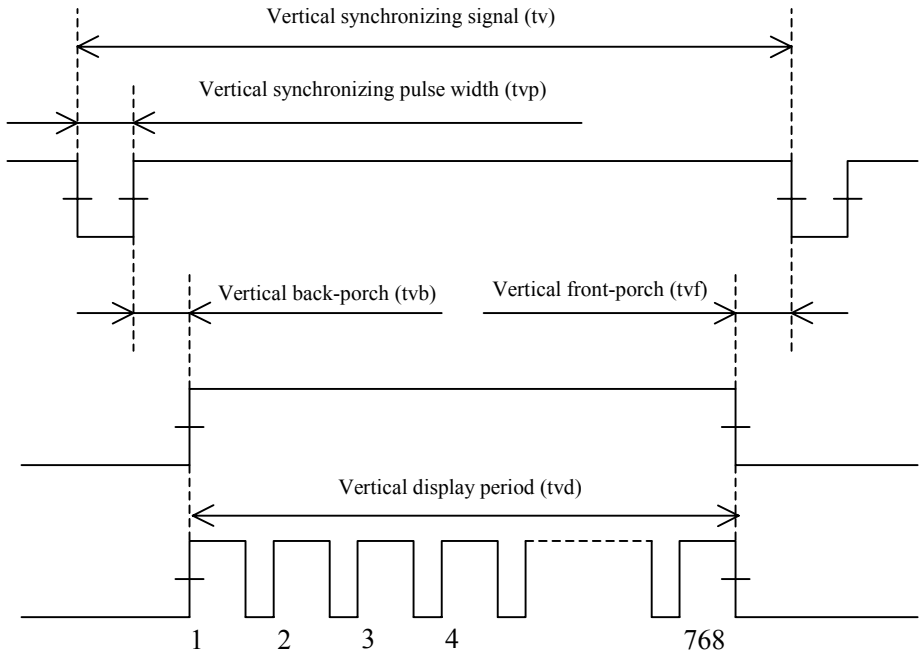
Odd Pixel: RA= R DATA Even Pixel : RB=R DATA
Odd Pixel: GA= G DATA Even Pixel : GB=G DATA
Odd Pixel: BA= B DATA Even Pixel : BB=B DATA

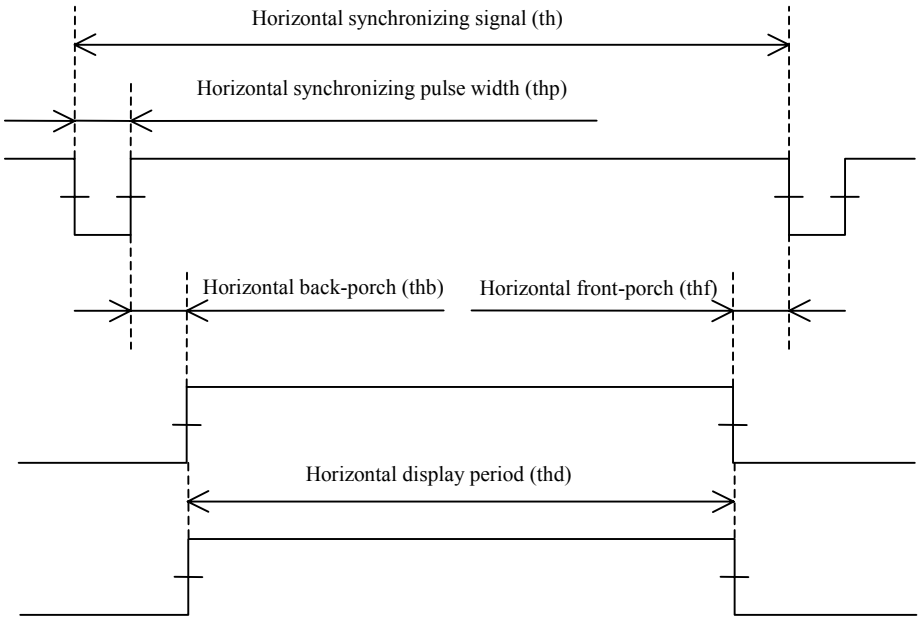


D(1, 1)	D(2,1)	•••	D(1024,1)
D(1,2)	D(2, 2)	•••	D(1024,2)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(1,768)	D(2,768)	•••	D(1024,768)

4.9 INPUT SIGNAL TIMINGS

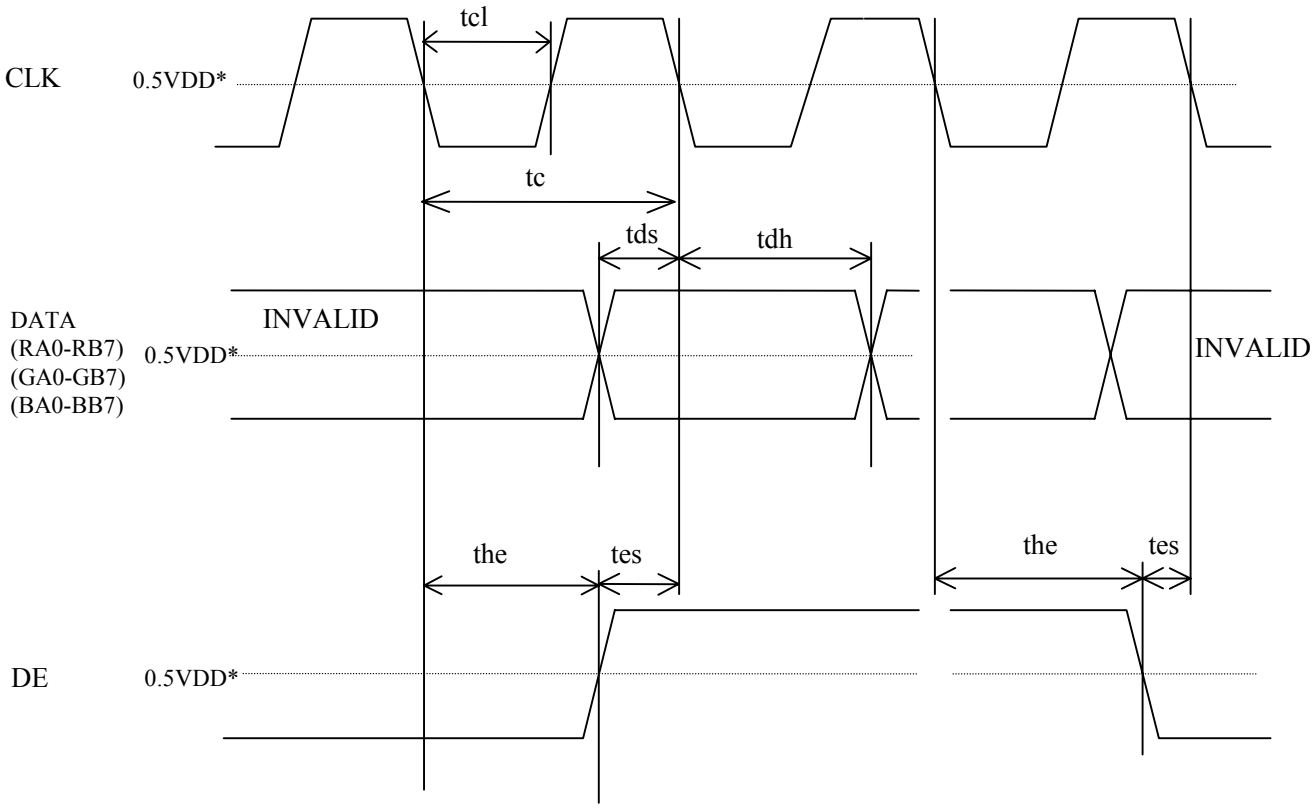
4.9.1 Definition of input signal timings



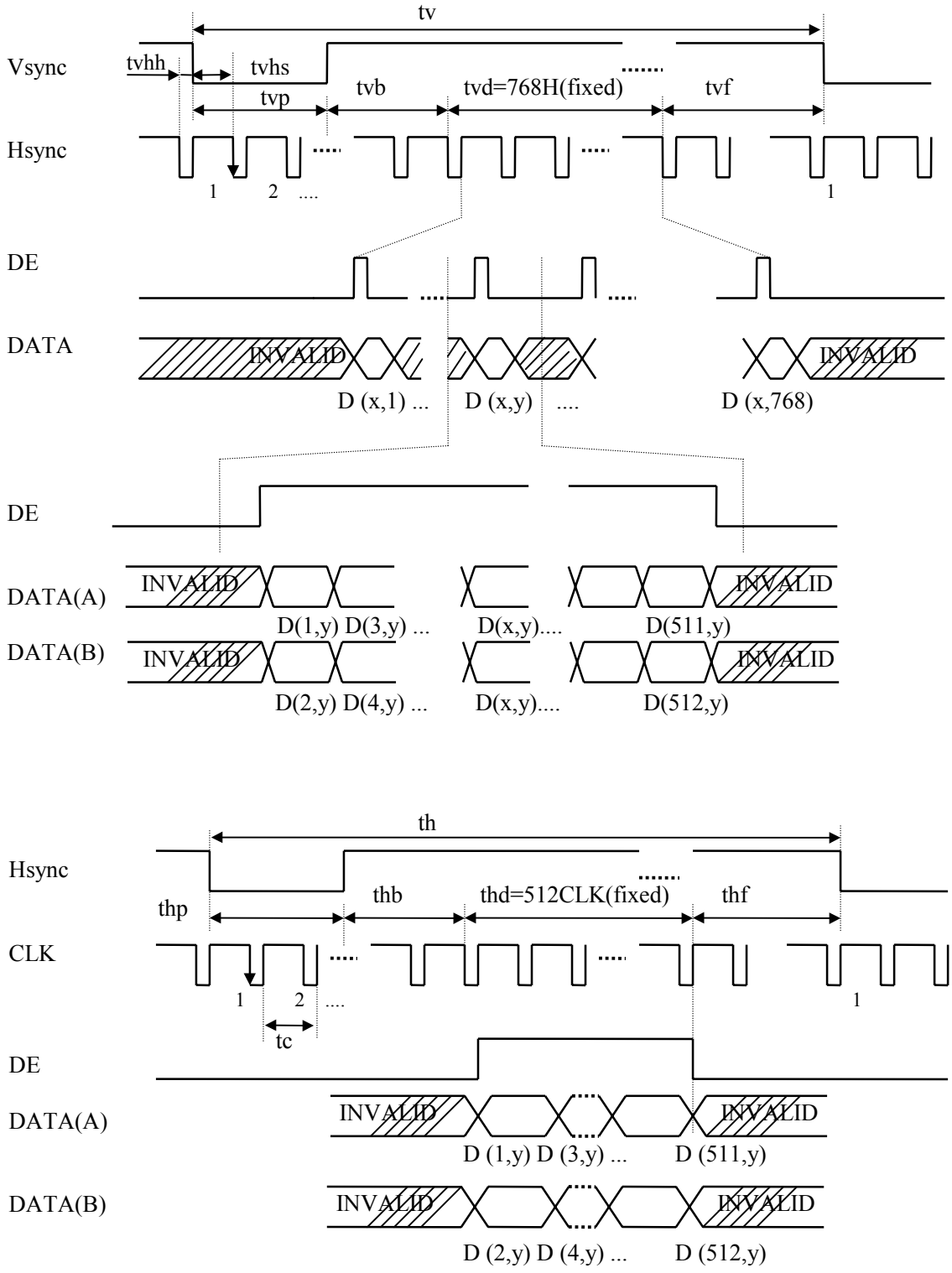


Note1: See "**4.9.4 Detailed input signal timing chart for numeration of pulse**".
Note2: These diagrams indicate virtual signal for set up to timing.

4.9.2 General input signal timing chart



4.9.3 Detailed input signal timing chart



DATA(A): RA0-RA7, GA0-GA7, BA0-BA7
DATA(B): RB0-RB7, GB0-GB7, BB0-BB7

4.9.4 Timing characteristics (2 port input)

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	Vf=75Hz	1/ tc	TBD -	39.375 25.397	TBD -	MHz ns	-
		Vf=60Hz		TBD -	32.500 30.769	TBD -	MHz ns	
	Duty		tcl / tc	0.4	0.5	0.6	-	-
Hsync	Period	Vf=75Hz	th	(12.3) (550)	16.660 656	- (1000)	μs CLK	Typ.=60.023kHz
		Vf=60Hz		(12.3) (550)	20.677 672	- (1000)	μs CLK	Typ.=48.363kHz
	Display period		thd	-	512	-	CLK	-
	Front-porch	Vf=75Hz	thf	-	8	-	CLK	-
		Vf=60Hz		-	12	-		
	Pulse width	Vf=75Hz	thp *	-	48	-	CLK	-
		Vf=60Hz		-	68	-		
	Back-porch	Vf=75Hz	thb *	-	88	-	CLK	-
		Vf=60Hz		-	80	-		
	* thp + thb			(38)	-	-	CLK	-
Vsync	Period	Vf=75Hz	tv	- (771)	13.328 800	TBD -	ms H	Typ=75.029Hz
		Vf=60Hz		- (771)	16.666 806	TBD -	ms H	Typ=60.0Hz
	Display period		tvd	-	768	-	H	-
	Front-porch	Vf=75Hz	tvf *	-	1	-	H	-
		Vf=60Hz		-	3	-		
	Pulse width		tvp *	-	3	-	H	-
				-	6	-		
	Back-porch		tvb *	-	28	-	H	-
				-	29	-		
	* tvp + tvb +tvf			(3)	-	-	H	-
	Vsync-Hsync timing		tvhs	1	-	-	CLK	-
	Hsync-Vsync timing		tvhh	1	-	-	CLK	-
DATA (RA0-RB7) (GA0-GB7) (BA0-BB7)	DATA-CLK (Set up)		tds	(2)	-	-	ns	-
	CLK-DATA (Hold)		tdh	(2)	-	-	ns	-
DE	DE-CLK timing		tes	(2)	-	-	ns	-
	CLK-DE timing		the	(2)	-	-	ns	-

Note1: All parameters should be kept within the specified range. Also Definition of unit is as follows.
1CLK = tc
1H = th

4.10 OPTICAL CHARACTERISTICS

(Ta= 25°C, VDD= 5V, VDDB=12V, Note1)

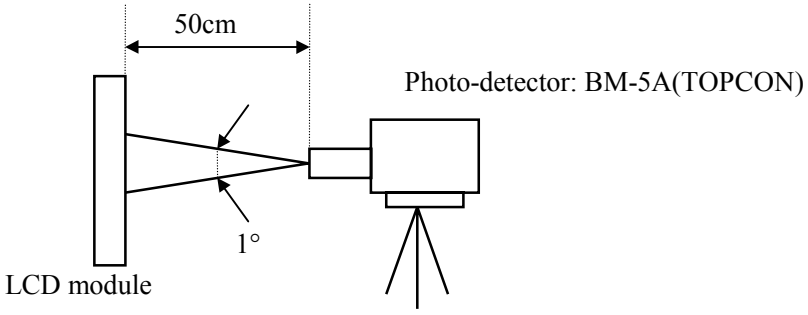
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	Note 3	(250)	300	-	-	Note2
Luminance	Lumax	Note 3	(300)	400	-	cd/m^2	-
Luminance uniformity	-	Max. / Min.	-	(1.1)	1.3	-	Note3,6
Chromaticity coordinates	W	White (x, y)	-	(0.300, 0.315)	-	-	Note3
	R	Red (x, y)	-	TBD	-	-	
	G	Green (x, y)	-	TBD	-	-	
	B	Blue (x, y)	-	TBD	-	-	

Reference data

(Ta= 25°C, VDD= 5V, VDDB=12V, Note1)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Color gamut		C	To NTSC	50	60	-	%	Note3
Viewing angle (CR>10)	Horizontal	θx+	CR>10, θy = ±0°	70	85	-	deg.	Note4
		θx-		70	85	-	deg.	
	Vertical	θy+	CR>10, θx = ±0°	70	85	-	deg.	
		θy-		70	85	-	deg.	
Viewing angle (CR>5)	Horizontal	θx+	CR>5, θy = ±0°	-	85	-	deg.	
		θx-		-	85	-	deg.	
	Vertical	θy+	CR>5, θx = ±0°	-	85	-	deg.	
		θy-		-	85	-	deg.	
Response time (Module front surface temperature = TBD°C)		Ton	Black to white: 10%→90%	-	(10)	(30)	ms	Note3,5
		Toff	White to black: 90%→10%	-	(10)	(20)		
Luminance control range		-	Maximum luminannce:100%	-	30-100	-	%	-

Note1: Optical characteristics are measured after 20 minutes from the module works. The typical value is measured after luminance saturation. The luminance is measured in dark room.
Input signal timing: XGA-60Hz mode

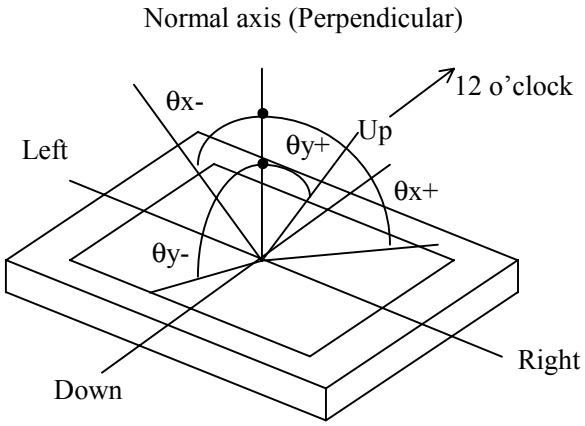


Note2: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in white}}{\text{Luminance with all pixels in black}}$$

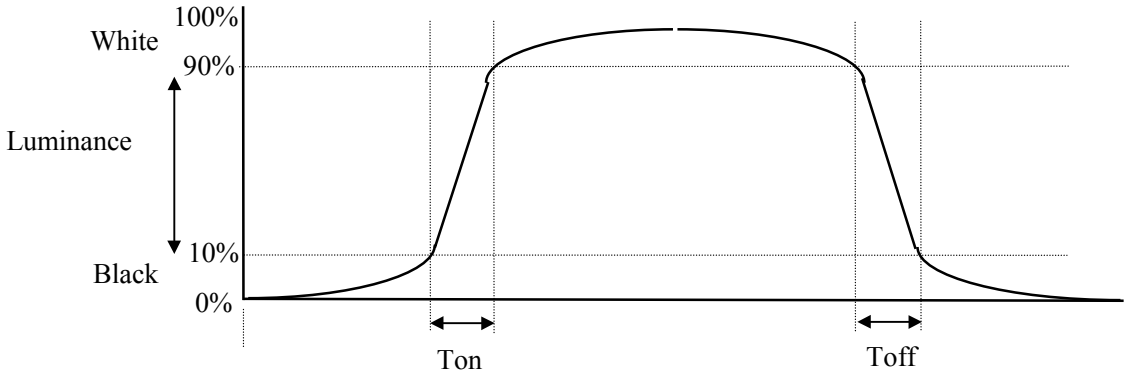
Note3: Viewing angle is θx = ±0°, θy = ±0° and at center.

Note4: Definitions of viewing angles are as follows



Note5: Definitions of response times are as follows.

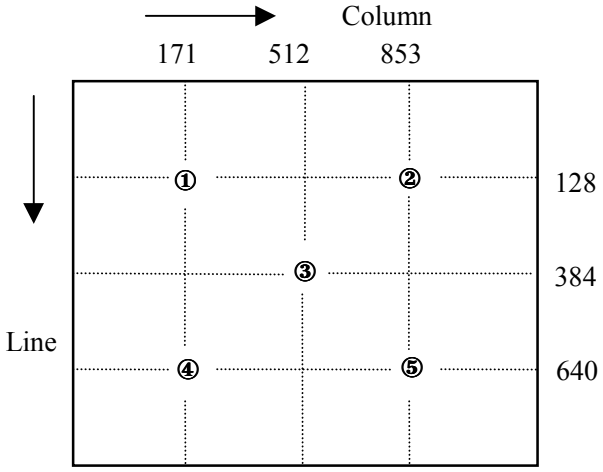
Response time is measured by photo-detector's out put level, when the luminance changes "black" to "white", or " black " to " white " on the same screen point. Ton is the time it takes the luminance to go from 10% to 90% on condition. Toff is the reverse of Ton (See the following diagram)



Note6: Luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

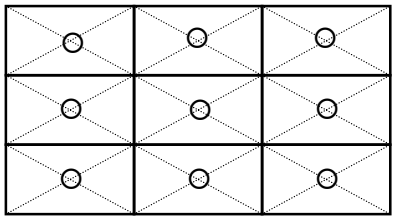
The luminance is measured at near the five points shown below.



5. RELIABILITY TEST

Test item		Test condition	Judgment
High temperature/humidity operation		60±2°C, RH=60% 240 hours, Display data is white.	Note1
Heat cycle (operation)		① 0°C ±3°C…1 hour 55°C ±3°C…1 hour ② 50 cycles , 4 hours/cycle ③ Display data is white.	Note1
Thermal shock (non-operation)		① -20°C ±3°C…30 minutes 60°C ±3°C…30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	Note1
Vibration (non-operation)		① 5-100Hz, 11.76m/s^2, 1 minute/cycle, X,Y,Z direction ② 10 times each direction	Note1, Note2
Mechanical shock (non-operation)		① 294m/s^2, 11ms X,Y,Z direction ② 3 times each direction	Note1, Note2
ESD (operation)		150pF, 150Ω, ±10kV 9 places on a panel *3 10 times each place at one-second intervals	Note1
Dust (operation)		15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	Note1
Low pressure	operation	53.3 kPa 0°C±3°C … 24 hours 55°C±3°C … 24 hours	Note 1
	non-operation	15 kPa -20°C ±3°C --- 24 hours -60°C±3°C --- 24 hours	

Note1: No display malfunctions (Display functions are checked under the same conditions as out-going inspection.)
Note2: Physical damage
Note3: See the following figure for discharge points.



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to understand following contents, respectively.**

⚠CAUTION	This sign has a meaning that customer will be injured himself and/or the module will sustain a damage, if he makes a mistake in operations.

This sign has a meaning that customer will get an electric shock if he makes a mistake in operations.

This sign has a meaning that customer will be injured himself if he makes a mistake in operations.

6.2 CAUTIONS

Do not touch HIGH VOLTAGE PART of the inverter while turn on. Customer will be in danger of an electric shock.

∗ Pay attention to handling for the working backlight. It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight. There will be in danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 (30G) and to be not greater 11ms, Pressure: To be not greater 19.6N (2kgf))

6.3 ATTENTIONS

(1) Handling the product

① When customer pulls out products from carton box, take hold of both ends without touch the circuit board. If customer touches it, products may be broken down and/or out of adjustment, because of stress to mounting parts.

② If customer places products temporarily, turn down the display side and place on a flat table.

③ Handle products with care and avoid electrostatic discharge (e.g. Decrease with earth band, ionic shower, etc.), because products (LCD modules) may be damaged by electrostatic.

④ The torque for mounting screws should never exceed 0.39N·m. Over torque may cause mechanical damage to the product.

⑤ Do not press or friction, because LCD panel surface is sensitive. If customer will clean the product surface, NEC Corporation or their supplier will recommend using the cloth with ethanolic liquid.

⑥ Do not push-pull the interface connectors while turn on, because wrong power sequence may break down the product.
⑦ Connection cables such as flexible cable, and so on, are danger of damage. Do not hook cables nor pull them.

(2) Environment
① Dewdrop atmosphere must be avoided.
② Do not operate and/or stores in high temperature and/or high humidity atmosphere. If customer store the product, keep in antistatic pouch in room temperature, because of avoidance for dusts and sunlight.
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ Use an original protection sheet on product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color and/or properties of the polarizer.

(3) Specification for products
① Do not display the fixed pattern for a long time because it may cause image sticking. If the fixed pattern is displayed on the screen, use a screen saver.
② The product may be changed of color by viewing angle because of the use of condenser sheet for backlight unit.
③ The product may be changed of luminance by voltage variation, even if power source applies recommended voltage to backlight inverter.
④ Optical characteristics may be changed by input signal timings.

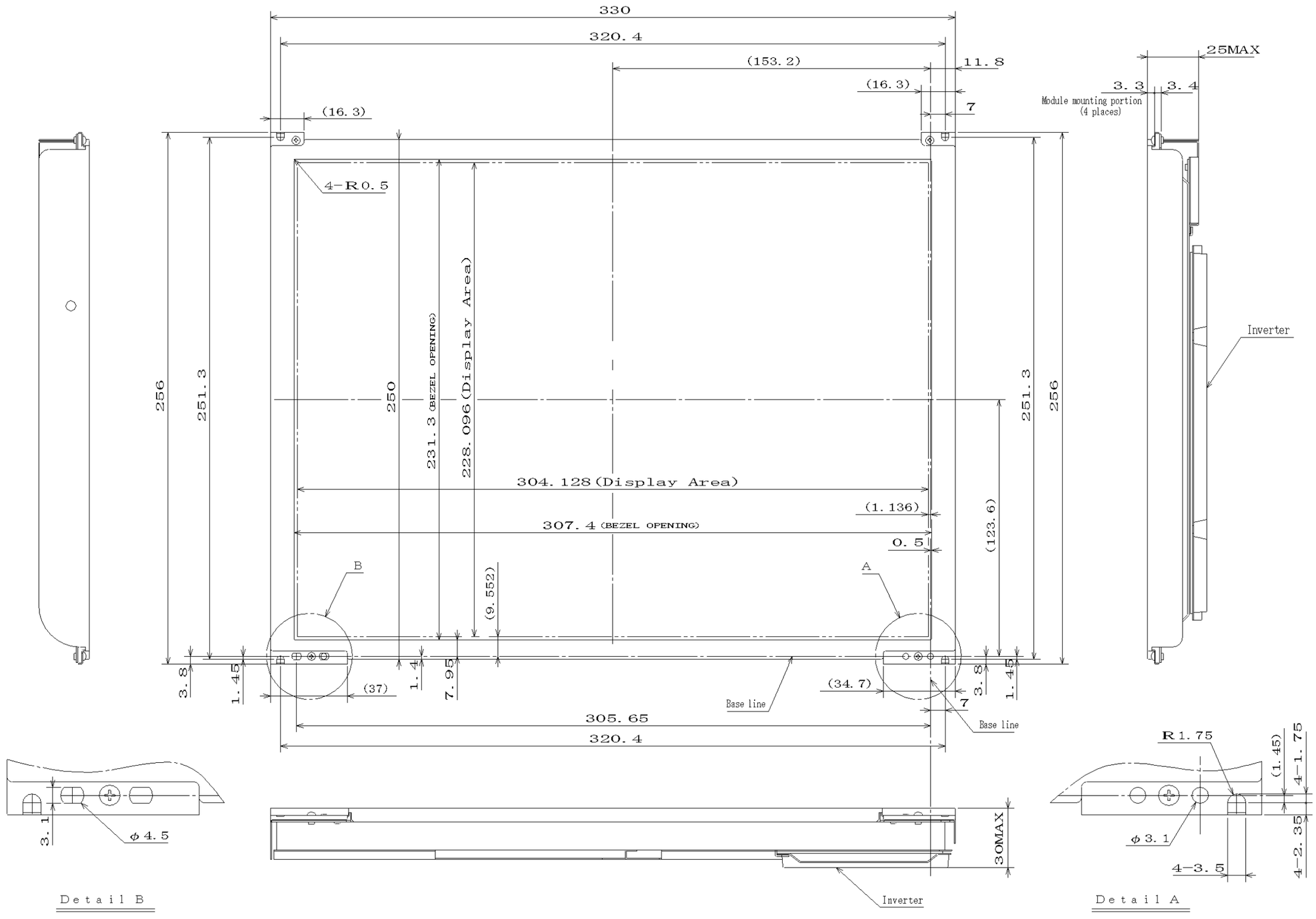
(4) Other
① All GND, GNDB, VDD and VDDB terminals should be connected without a non-connected signal line.
② Do not disassemble a product and/or adjust volume.
③ If customer would like to replace backlight lamps, see 'REPLACEMENT MANUAL FOR BACKLIGHT'.
④ If customer use screwnails, pay attention not to insert waste materials in inside of products.
⑤ When customer returns product for repair and so on, pack it with original shipping package because of avoidance of some damages during transportation.

General specifications for the LCD
The following items are neither defects nor failures.

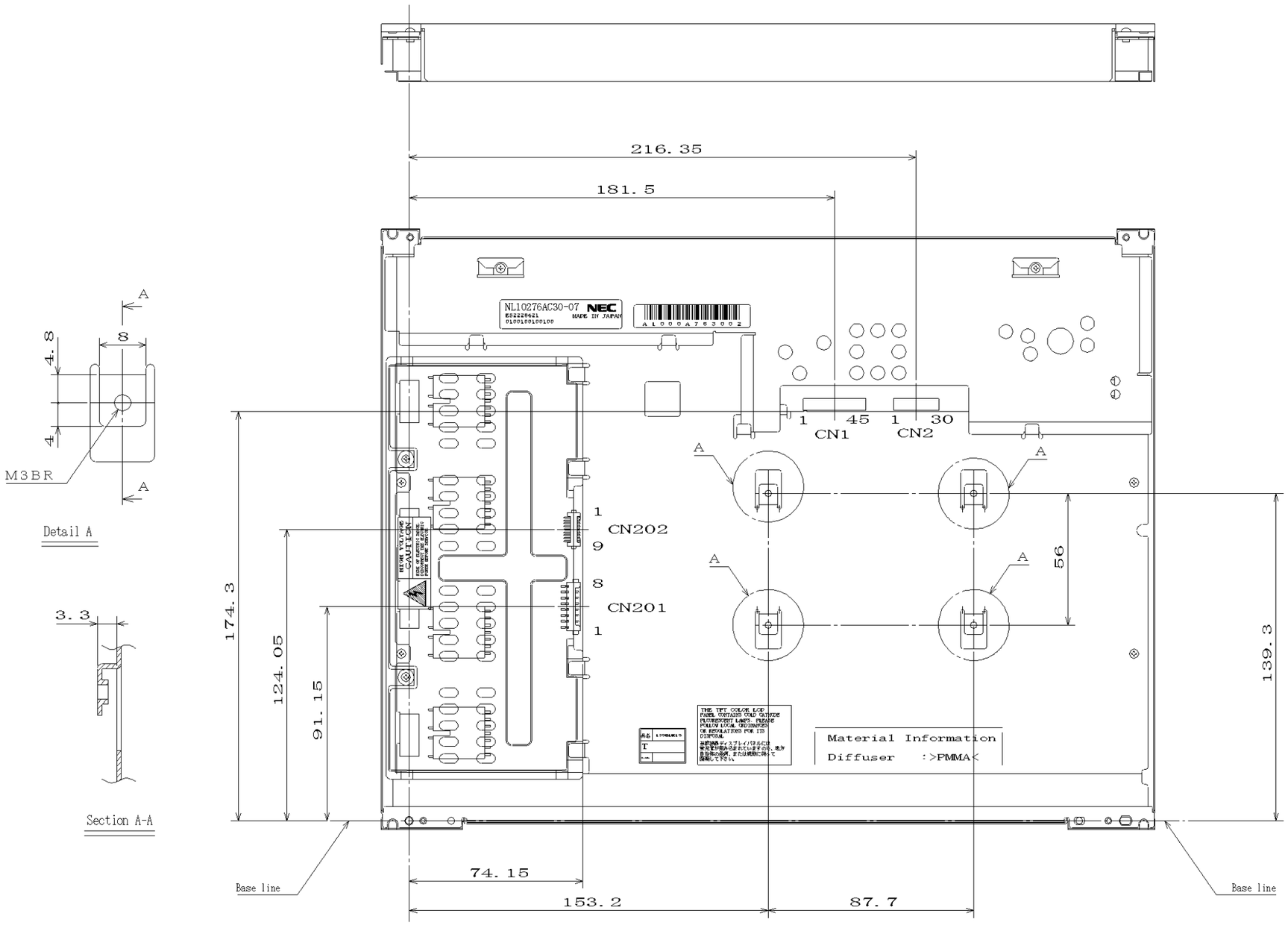
∗ Response time, luminance and color gamut may be changed by ambient temperature.
∗ The LCD may be seemed luminance uniformity, flicker, vertical seam and/or small spot by display patterns.
∗ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.

7. OUTLINE DRAWINGS(Unit: mm)

7.1 Front view



7.2 Rear view


216.35
181.5
NL10276AC30-07 NEC
MADE IN JAPAN
1 45 1 30
CN1 CN2
1
CN202
9
8
CN201
1
174.3
124.05
91.15
56
139.3
74.15
153.2
87.7
Base line
Base line
A
4.8
8
4
M3BR
Detail A
3.3
Section A-A
THE TFT COLOR LCD PANEL CONTAINS COLD CATHODE FLUORESCENT LAMP. PLEASE FOLLOW LOCAL ORDINANCES OR REGULATIONS FOR ITS DISPOSAL.
Material Information
Diffuser :>PMMA<

Revision History

Rev.	prepared date	Revision contents	**Signature of writer**
1st edition	Jan. 25, 2001	DOD-M-0094(abstract)	*Approved by* A. OKAMOTO *Checked by* ——— *Prepared by* R.KAWASHIMA
2nd edition	Feb. 6, 2001	DOD-M-0140(abstract) P5 Outline of characteristics: Expression of viewing angle is revised. P7,8 Symbols: VCC→VDD, ICC→ IDD (correction) P7 ABSOLUTE MAXIMUM RATINGS: VDD is corrected. P14 (4) Luminance control: Expression of remark is revised. P15 Symbols: Luminance→Luminance ratio (correction) P23 Vibration: 50 times→10 times (collection) ESTIMATED LIFE TIME OF THE BARE LAMP is deleted.	*Approved by* A. OKAMOTO *Checked by* ——— *Prepared by* R.KAWASHIMA
3rd edition	Mar. 30, 2001	DOD-M-0276 Change part (Before-2nd edition → After-3rd edition) The inside of this document is revised the clerical error and unclear expression in previous one. The important changes such as specifications, characteristics and functions are as follows. P5,P7,P28 Module size (Vertical): 255.4mm→256.0mm P6 BLOCK DIAGRAM-Vertical resolution: 1024→768 P7 ABSOLUTE MAXIMUM RATINGS •VDDB: -0.3 to +16.0V → -0.3 to +15.0V •ACA is added. • Absolute humidity: Absolute humidity shall not exceed Ta=50°C, Relative humidity =70% level. → ≤ 78 g/m^3 P8 Driving for backlight inverter •Logic input voltage is added. •ACA is added. P13 Backlight inverter- CN202 socket-Pin No.2: N.C. →ACA P18 Definition of input signal timings are added. P24 RELIABILITY TEST: Low pressure is added. P27,P28 OUTLINE DRAWINGS are revised.	*Approved by* A. OKAMOTO *Checked by* ——— *Prepared by* R.KAWASHIMA

Revision History

Rev.	prepared date	Revision contents	**Signature of writer**
4th edition	June 12, 2001	DOD-M-0433 Change part (Before-3rd edition → After-4th edition) The inside of this document is revised the clerical error and unclear expression in previous one. The important changes such as specifications, characteristics and functions are as follows. P4 Applications: PC monitor is deleted. P5, P7, P28 Module thickness: 32.0mm Max. → 30mm Max. P5, P7 Module weight: 1200g Typ., TBD Max. → 1100g Typ., 1200g Max. P5, P23 Contrast ratio is decided. P5, P23: Luminance is decided. P6 Block diagram: Note1 is changed. P7 Absolute maximum ratings BRTP, PWSEL, ACA, BRTL, Operating altitude and Storage altitude: Each parameter is decided. P8 Electrical characteristics IDD, BRTC, BRTP, PWSEL, ACA and BRTL: Each parameter is decided. P9 Luminance control frequency is decided. P9 Fuses are decided. P10 Sequence for LCD panel signal processing board is decided. P11 CN1 socket: "FH12S-45S-0.5SH (HIROSE)" is added. Adaptable plug is deleted. P12 CN2 socket: "FH12S-30S-0.5SH (HIROSE)" is added. Adaptable plug is deleted. Note2 is added. P28, P29: Outline drawings are changed.	*Approved by* *Checked by* *Prepared by* R. Kawashima